Breaking the IGBT E_{loss}/V_{CEsat} trade off relationship by wedding Si IGBT + SiC MOSFET

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Abstract

In this paper hybrid switches consisting either of high speed or low V_{CEsat} Si IGBTs, connected in parallel with low current SiC MosFET, have been proposed as a novel approach to combine the best features of Silicon IGBTs and Silicon Carbide MosFET switches at the lowest possible costs. The requirements for lower losses and higher switching frequencies has led to the development of SiC devices, but their higher cost has slowed their adoption. In addition to the significant acceleration in switching speed, the SiC MosFET is able to lower the V_{CEsat} and enables freewheeling through its body diode.

1 Introduction

Si IGBTs are being widely used in power applications as they are rugged, widely available from several sources and affordable. The newly emerging SiC MosFETs are fulfilling todays application requirements [1]. Unfortunately, due to their higher cost they are being unable to fully replace Si IGBTs. Therefore, the hybrid switch has been proposed, which is a well investigated concept in terms of SiC MosFET cost, current ratios, influence by external parameters, gate control and others. [2][3][4].

From the perspective of IGBTs there is a trade-off relationship between the required switching speed of the device and its on-state voltage drop V_{CEsat}. Ever more efforts are spent to increase its performance which increases its complexity and reduces its ruggedness. As turn-on losses are dominated by co-packed or external freewheeling diodes (FWD), replacement of Silicon with SiC Diodes have become quite popular. In this paper the authors follow the path towards the perfect switch by tuning the IGBT for lowest conduction loss while replacing the FWD with a miniature sized SiC MosFET at similar cost of its SiC Diode counterpart, overcoming the IGBT trade-off relationship by significantly reducing the switching-losses and enabling free-wheeling functionality.

Analysis of the static and dynamic behavior in a half-bridge topology of the different H-SW will be performed, using 950 V Si IGBTs at various trade-off points in parallel with 900 V 60 mOhm SiC MosFET. This will be compared with common silicon and silicon carbide co-pack solutions.

1.1 The hybrid switch

The proposed H-SW switches are shown in Fig. 1, where one switch consists of a low V_{CEsat} Si IGBT paralleled with a SiC MOSFET and the other one combines a fast Si IGBT with the same SiC MOSFET. The two IGBTs are available from ON Semiconductor, Trench Field Stop 4th generation.

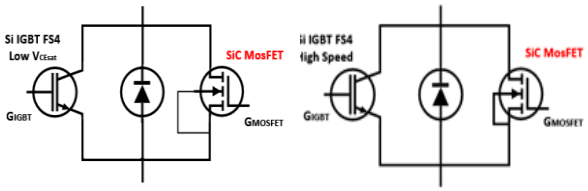


Fig. 1: H-SW configuration a) Low V_{CEsat} IGBT b) High Speed IGBT

The low V_{CEsat}=1.3 V Si IGBT was designed for high performance power conversion application, where the low conduction losses are crucial. On the other hand, the fast IGBT shows higher V_{CEsat}= 1.7 V. It was optimized for higher frequency operation and reduced switching losses.

Figure 2 shows the improvement in V_{CEsat} at 25°C by introducing the H-SW. Due to the immediate conduction through the SiC MosFET at low

voltage, the hybrid device demonstrates a significant lower voltage drop hence lower conduction losses. Due to the low gate charge, the MosFET responds immediately and consequently turn-on losses are dramatically reduced.

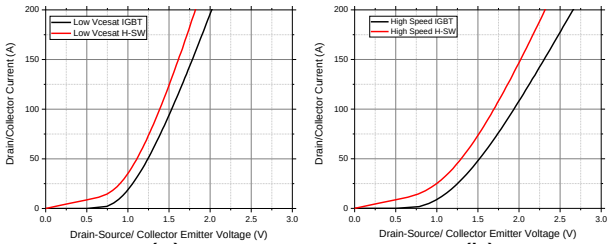


Fig. 2: I-V characteristic a) High speed IGBT vs high speed H-SW b) Low V_{CEsat} IGBT vs low V_{CEsat} H-SW

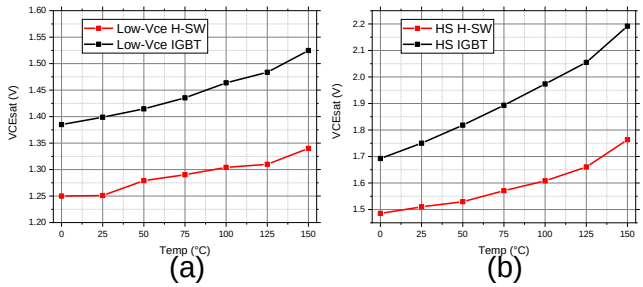


Fig. 3: V_{CEsat} (at Ic/d= 75 A) change over temperature (0°C-150°C, 25°C steps a) Low V_{CEsat} IGBT vs Low V_{CEsat} H-SW b) High speed IGBT vs High speed H-SW

Additionally, the losses at higher operating temperature are reduced as well with the H-SW. The V_{CEsat} behavior over temperature is shown in Fig.3 for the single IGBT's and the H-SW.

The H-SW reduces V_{CEsat} at 25C by 10 to 15%. At elevated temperatures this effect amounts to 15-20% respectively.

2 Comparison of total loss between IGBT and H-SW

2.1 Double Pulse Tester

In order to show the losses improvement from the proposed switches, a double pulse tests has been performed with a clamed inductive load – a half-bridge configuration with symmetric device on the high and low side. Figure 4 shows the test setup.

Dynamic tests are performed with the proposed IGBTs and H-SW, each of them being DUT. At this setup, the turn-on and turn-off losses shown in Fig. 6 and Fig. 7 are measured.

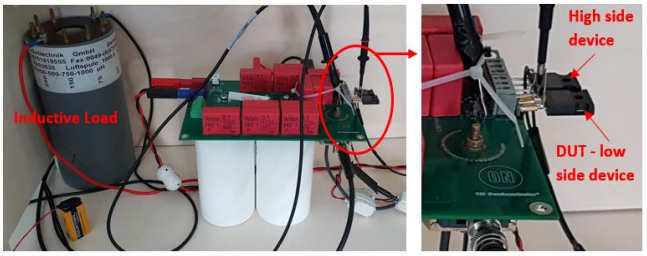


Fig. 4: Hardware of a the double pulse tester with an clamed inductive load;

Both the SiC MosFET and the Si IGBT are integrated in the same TO-247 3L package. For driving the H-SW, an IGBT gate driver is being used, without introducing any additional delays for driving the gates of the Si IGBT and SiC MosFET. In this way, additional costs are avoided for optimization of the gate drive and control – offering simple drop-in solution.

2.2 Analysis of the influence of the H-SW on switching losses

2.2.1 Impact on the E_{ON} losses

The switching losses during on-transition significantly reduced when compared the IGBT to the H-SW. This could be seen from the comparison of the waveforms during on transition shown in Fig. 5.

During on transition, the DUT starts conducting the current when the V_{TH} is reached. At the same time, the FWD on high side changes from conduction state to non-conducting. The FWD conducts temporarily in reverse direction, which is added to the steady state current delivered by the load. The overlap of high voltage $V_{DS/CE}$ and high current $I_{D/C}$ is causing the E_{ON} losses.

Equation (1) describes the relationship for calculating the E_{ON} losses. The lower the $I_{D/C}$ current peak, the shorter the time and smaller the losses.

$$E_{sw\_ON} = \int_{t_{sw,on}} V_{CE} I_C dt \qquad (1)$$

On the other hand, the H-SW turn-on transitions are much faster. As seen in Fig. 2, the Si IGBT has a dead time until it starts conducting at low voltage, where the H-SW uses the low capacitances of the

SiC MosFET and instantaneously conducts the current.

The $V_{DS/CE}$ voltage speed for the high speed H-SW has been improved by 34%, where the HS IGBT dV/dt_{IGBT}= 16.87 V/ns and HS H-SW $dV/dt_{HSHybrid}$= 22.76 V/ns.

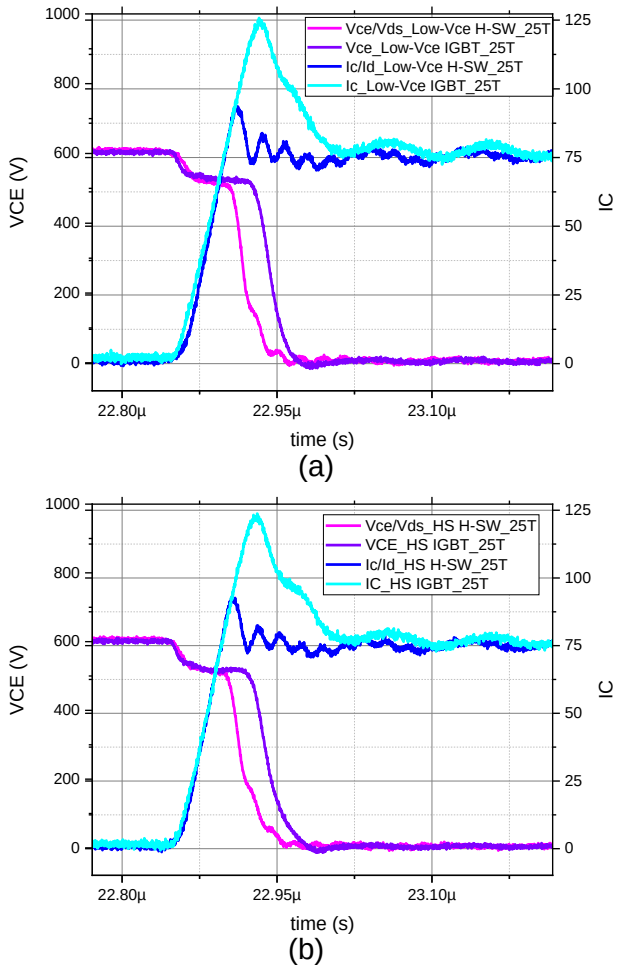


Fig. 5: Turn-on waveforms at 600 V 75 A ($V_{GE/GS}$= 15 V/ -8 V) for: a) Low V_{CEsat} IGBT vs low V_{CEsat} H-SW b) High speed IGBT vs high speed H-SW

The $V_{DS/CE}$ voltage transient for the Low-V_{CEsat} H-SW was improved by 32%, where the Low-V_{CEsat} IGBT dV/dt_{IGBT}= 20.2V/ns and Low-V_{CEsat} H-SW $dV/dt_{LSHybrid}$= 26.9 V/ns.

The $I_{D/C}$ current transient for the high speed H-SW was improved by 10%, where the HS IGBT dI/dt_{IGBT}= 1.68 A/ns and HS H-SW $dI/dt_{HSHybrid}$= 1.84 A/ns. The $I_{D/C}$ current transient for the low -V_{CEsat} H-SW was improved by 22%, where the Low-V_{CEsat} IGBT dI/dt_{IGBT}= 1.68 A/ns and LS H-SW $dI/dt_{LSHybrid}$= 1.84 A/ns.

Base on this result, we observe 50% E_{ON} losses reduction with the H-SW at the nominal rated current of the device. The same result can be observed at elevated temperatures.

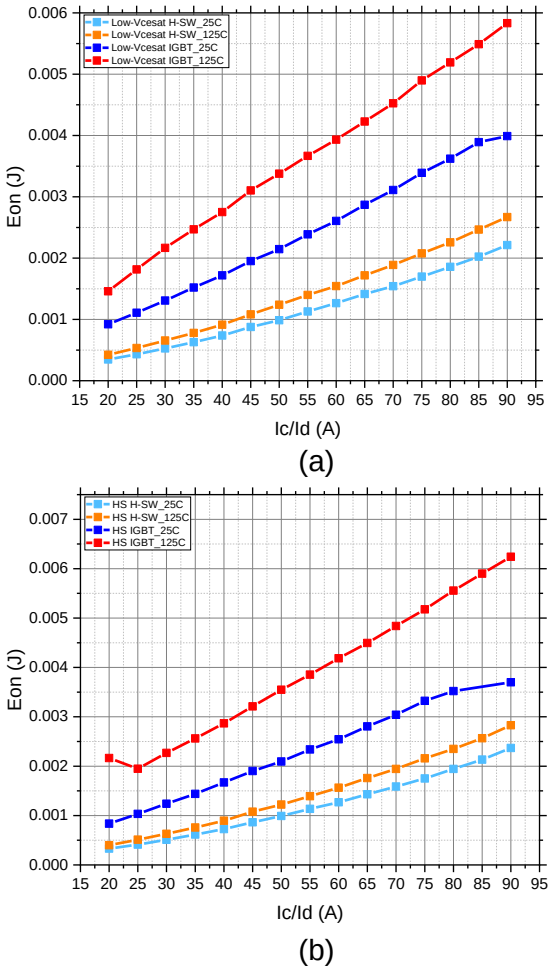


Fig.6: a) Comparison of E_{ON} losses over current between Low-V_{CEsat} IGBT (E_{ON} losses at 25°C – blue, E_{ON} losses at 125°C – red) and Low-V_{CEsat} H-SW (E_{ON} losses at 25°C – light blue, E_{ON} losses at 125°C – orange); b) Comparison of E_{ON} losses over current between high speed IGBT (E_{ON} losses at 25°C – blue, E_{ON} losses at 125°C – red) and high speed H-SW (E_{ON} losses at 25°C – light blue, E_{ON} losses at 125°C – orange);

2.2.2 SiC Body Diode compared to Si Diode

The benefit of the low reverse recovery of the SiC body diode from the SiC MosFET has been demonstrated in the waveforms shown in Fig. 5. Now the reverse recovery losses of the both Si and SiC diode will be compared.

The energy dissipated due to the significant reverse recovery losses of the Si Diode is shown in Fig.7. We observe ~75% lower switching losses

due to the SiC body diode at room temperature and ~80% at higher temperatures.

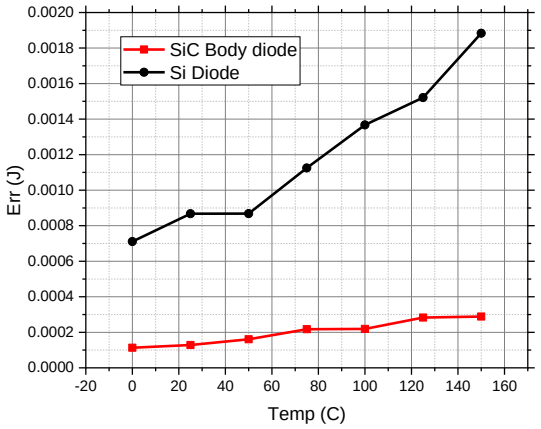


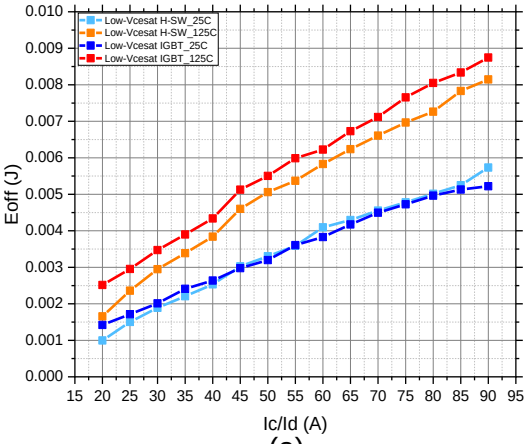
Fig.7: Reverse recovery energy losses of the SiC body diode (red) and Si Diode (black) over temperature at 600 V and $I_{C/D}$=75 A

2.2.3 Impact on the E_{OFF} losses

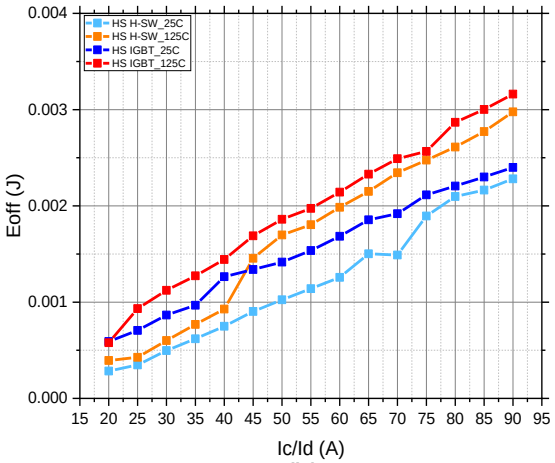
The switching losses during off transition are not being influenced by the H-SW. As there is no delay included in the driving of the H-SW, the IGBT and the SiC MosFET are switching off at the same time point and the tail current of the IGBT stays present.

$$E_{sw\_OFF} = \int_{t_{sw,off}} V_{CE} I_C dt \qquad (2)$$

The calculation of the E_{OFF} losses is shown in Eq. (2) and the comparison results in Fig. 8 are showing the very little change in E_{OFF} losses.



(a)



(b)

Fig. 8: a) Comparison of E_{ON} losses over current between Low V_{CEsat} IGBT (E_{ON} losses at 25°C – blue, E_{ON} losses at 125°C – red) and Low V_{CEsat} H-SW (E_{ON} losses at 25°C – light blue, E_{ON} losses at 125°C – orange);
b) Comparison of E_{OFF} losses over current between high speed IGBT (E_{OFF} losses at 25°C – blue, E_{OFF} losses at 125°C – red) and high speed H-SW (E_{OFF} losses at 25°C – light blue, E_{OFF} losses at 125°C – orange);

2.3 Total switching and conduction power losses analysis based on application level

From the double pulse testing in the previous chapter, a detailed analysis of the switching losses over different current loads and temperatures has been conducted.

For the analysis of the conduction losses and total losses, a typical motor drive inverter application is considered. It is assumed continuous operation of the devices at a switching frequency of 20 kHz and 50% duty cycle for the high speed Si IGBT and H-SW and switching frequency of 10 kHz and 50% duty cycle for the low V_{CEsat} Si IGBT and H-SW. In following, the power losses would refer to a losses for one period.

Though the devices are rated at higher current, in a real application the operating peak current is much lower. In this case all the power losses are calculated at peak current 25 A.

2.3.1 Impact on the conduction losses

The conduction losses are caused by the $I_{D/C}$ current flow through the device and the saturation voltage (on state voltage) during the conduction period, as explained in Eq. (3).

$$P_{cond} = D * \int_{t_{sw,on}} V_{CE(on)} I_C dt \quad (3)$$

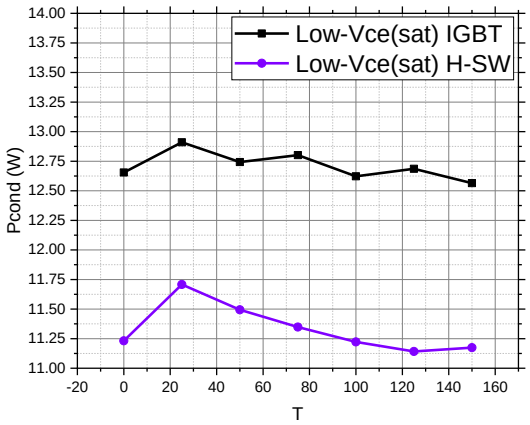


Fig. 9: Conduction power losses over temperature at $I_{C/D}$= 25 A over temperature for low-V_{CEsat} Si IGBT (black) vs low-V_{CEsat} H-SW (purple);

The conduction losses for the low-V_{CEsat} Si IGBT are 10% higher than the H-SW, shown in Fig. 9. The same trend is observed also at higher temperatures.

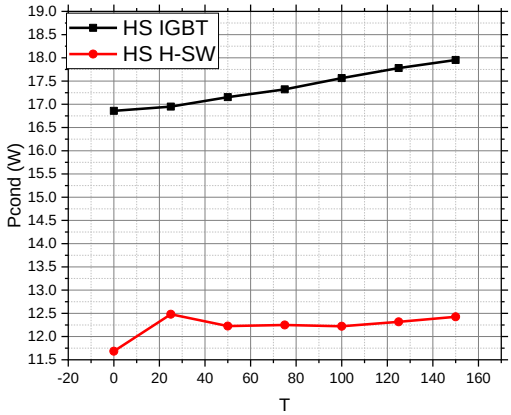


Fig. 10: Conduction power losses over temperature at $I_{C/D}$= 25 A over temperature for high speed Si IGBT (black) vs high speed H-SW (red);

On the other hand, the conduction losses of the high speed Si IGBT and H-SW are showing significant larger reduction of conduction losses of 26%, whereas the high-temperature conduction losses of the H-SW show improvement up to 35% (see Fig. 10).

This is significant impact on the conduction losses with the H-SW solution proposed in this paper.

2.3.2 Total power losses overview on application level

A short overview follows to summarize the total power losses from an application point of view.

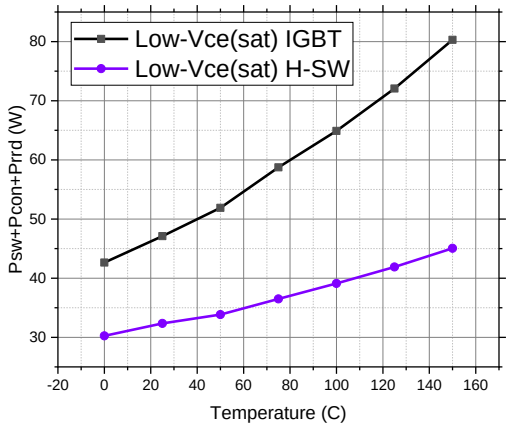


Fig. 11: Total power losses: Switching, reverse recovery and conduction power losses over temperature at $I_{C/D}$= 25 A over temperature for low-V_{CEsat} Si IGBT (black) vs low-V_{CEsat} H-SW (purple);

Based on the data presented in this paper (see Fig. 11), 38% decrease in the total power losses with the low-V_{CEsat} H-SW implementation at room and ~42% at high temperatures are achieved.

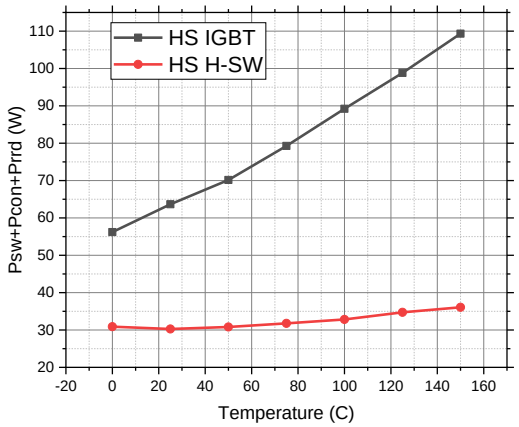


Fig. 12: Total power losses: Switching, reverse recovery and conduction power losses over temperature at $I_{C/D}$= 25 A over temperature for high speed Si IGBT (black) vs high speed H-SW (red);

The high speed H-SW is showing 52% decrease in the total power losses at room and ~63% at high temperatures (see Fig.12)

The impact percentage of the H-SW device on each of the power losses in an application is shown in Table 1.

Losses	Low-V_{CEsat} Si IGBT vs low-V_{CEsat} H-SW – difference in [%]	High speed Si IGBT vs high speed H-SW – difference in [%]
Switching	-33% (at 25°C)to -40%(150°C)	-55% (at 25°C)to -70%(150°C)
Conduction	-11% (at 25°C)to -12%(150°C)	-26% (at 25°C)to -35%(150°C)
Reverse Recovery	-75% (at 25°C)to -85%(150°C)	

Table 1: Power losses decrease in [%] when a H-SW is considered in an application;

The low-V_{CEsat} H-SW is improving the performance of the Si IGBT, by offering even lower conduction losses and meet the application requirements.

Whereas the high speed H-SW can offer even lower switching losses and lower conduction losses.

Finally, we can show the comparison of the E_{LOSSES}/V_{CEsat} trade-off curve for single Si IGBT and H-SW solution, see Fig. 13.

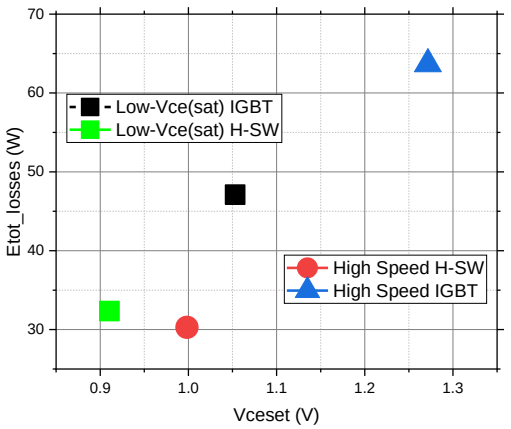


Fig. 13: Comparison of the E_{tot_loss}/V_{CEsat} trade-off curve for low-V_{CEsat} Si IGBT and H-SW and high speed Si IGBT and H-SW

2.4 Cost analysis of the H-SW

At the moment, the replacement of Si IGBTs by similar rated SiC MosFETs is a rather costly option, even though the applications can achieve much lower losses with its implementation.

Therefore, as an intermediate approach, the H-SW solution has been proposed. In this case the hybrid power device benefits from both technologies and for a much lower cost. On one side, the hybrid device shows better performance with the help of the SiC MosFET and on the other side the low reverse recovery of the SiC body diode.

The H-SW used in this investigation are estimated to increase the cost of the reference IGBT by 50%--250% depending on the used SiC MosFET die size.

As an outcome, the power losses are being decreased for 50%. For an application, 50% power losses decrease is quite significant.

3 Conclusion

In this paper, a novel H-SW with different trade-off points was analyzed as an intermediate approach before full adoption of full SiC MosFET solution.

Compared to the incumbent Si IGBT devices, the H-SW has demonstrated the superior performance and significant reduction of total losses. In particular turn-on and conduction losses are being significantly improved.

The H-SW is coming at affordable cost and easy to implement. For future work, it would be interesting to evaluate the hybrid solution for long term reliability at an application level.

4 References:

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